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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,512	02/17/2004	Chee Siong Lee	42P18829	2960

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EXAMINER	
UNELUS, ERNEST	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 08/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/781,512	LEE ET AL.	
	Examiner	Art Unit	
	Ernest Unelus	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-10* is/are allowed.

6)☒ Claim(s) *11-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
8/25/2006

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO AMENDMENT

A. Double Patenting Rejection

There was never a double patenting rejection done on this application (10/781,512). The applicant's remark for this applicant doesn't need a response on a double patenting rejection.

B. Claim Rejections Under 35 USC § 103

Applicant's arguments filed 07/21/2006 have been fully considered but they are not persuasive.

As per claim 1, the applicant amended claim 1 by including request after "incoming" and before "cycle"

In regards to the term "request cycles", paragraph 0003 from the applicant's specification discloses that the request cycle is "***generally***" two categories of cycles. The applicant's specification further stated **"i.e. *a write request cycle...*".** As stated in the applicant's specification, the request cycles is not only limited to the two categories. The examiner also points out that the two categories are not claimed.

As per claims 11, 16, and 21, the added limitation is not supported by all the choices. For example, in claim 16, the added limitation "wherein the control logic instructs the completion queue whether or not to return a completion packet associated with the modified non-posted cycle to the requesting device" is only applicable to "(2) modified header information associated with modified non-posted cycle"

II. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

1. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. INFORMATION CONCERNING DRAWINGS

Drawings

2. The applicant's drawings submitted are acceptable for examination purposes.

III. REJECTIONS NOT BASED ON PRIOR ART

3. The applicant's drawings submitted are acceptable for examination purposes.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 11, 16, and 21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. As per claims 11, 16, and 21, the added limitation is not supported by all the choices. For example, base on the specification, claims 11 and 21, the added limitation "instruction the completion queue whether or not to discard a completion packet received from a designated end-device" is only applicable to "(2) modified header information associated with

modified non-posted cycle" and " (3) header information associated with a new request cycle generated in response the received incoming". The specification does not support the added limitation for "(1) unmodified header information from the captured non-posted request cycle".

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 16 is also rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The added limitation is not supported by all the choices. The added limitation "wherein the control logic instructs the completion queue whether or not to return a completion packet associated with the modified non-posted cycle to the requesting device" is only applicable to "(2) modified header information associated with modified non-posted cycle".

IV. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

> The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bernasconi et al. (US pat. 6,158,018) in view of Hagan et al. (US pat. 6,158,018).

4. As per **claims 11 and 21**, Bernasconi discloses a method comprising: "receiving an incoming request cycle **(24)** from a requesting device **(16)**; determining if the received incoming request cycle matches one or more of preprogrammed trigger conditions **(col. 9, lines 51-57, teaches that the trigger-matching logic is the logic that doest the matching between the current DSP program address and a break address correspond to a flawed DSP program stored in the ROM 18, such as at section 18b)**; determining if the received incoming request cycle is a non-posted cycle **(the trigger-matching logic is automatically receiving "non-posted cycle". The "non-posted cycle" is request that need to be complete, as stated by the applicant in paragraph 0017)**; **Bernasconi also discloses**, "if the received incoming cycle matches a trigger condition and is a non-posted cycle **(col. 9, lines 51-57), the patching circuitry does** one of following (1) unmodified header information from the captured non-posted cycle **(see fig. 1 and col. 9, line 57 to col. 10, line 5)**, (2) modified header information associated with a modified non-posted cycle, or (3) header information associated with a new cycle generated in response the received incoming cycle.

Bernasconi fails to specifically teach specifying whether the I/O controller including a patch module **(patching circuitry22)** coupled to a completion queue is to be loaded with information from non-posted cycle. However, Hagan suggests interrupt state to be cleared when the entry is posted, the interrupt state being associated with each entry in the queue **(see abst. and col. 4, lines 47-59).**

Bernasconi's invention and Hagan's invention's are analogous art because they are from the same field of endeavor storing data into queue from a processor. In view of

such teaching, at the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the patch mechanism used to detect and workaround defects and conditions existing in an integrated circuit chip as taught by Bernasconi which includes a DSP and a patching circuitry that's consist of a trigger-matching logic, further include a control logic coupled to the trigger-matching logic is modified to include a completion queue to be loaded with information from non-posted cycle as taught by Hagan.

The motivation for doing so would have been because Hagan teaches that **["The significant instructions generally translate into increased processing time, slowing the response of the processor determining whether the current queue entry is empty. Therefore, it would be advantageous to have an improvement with an apparatus for reducing the processing overhead for multiple processor or embedded processor architectures in posting events or tasks to a queue"(col. 1, lines 49-56)]**.

Therefore, it would have been obvious to combine Hagan and Bernasconi for the benefit of creating a patch mechanism used to detect and workaround defects and conditions existing in an integrated circuit chip to obtain the invention as specified in claims 11 and 21.

5. As per **claims 12, 14, 22, and 24,** Bernasconi discloses "the method of claim 11,"**[see rejection to claim 11 above]** "wherein generating a modified non-posted, **which is a new request cycle**, in response to a matched trigger condition **(col. 9, lines 9, lines 57 to col. 10, line 5, teaches the that the control logic is taught by Bernasconi's patching circuitry 22, which**

carries out the steps of sending a branch op code to the DSP 16 followed by a branch address corresponding to the beginning of a block of corrected DSP program software in the RAM 20 such as in section 20b.); sending the modified non-posted cycle to a destination device **(processor 16 in fig. 1);** and discarding a completion associated with the new request cycle received from the destination device **(col. 10, lines 50-60)**.

6. As per **claims 13 and 23**, Bernasconi discloses "wherein the patch module can return a completion associated with the modified non-posted cycle to the requesting device **(16) (see fig. 1 and col. 9, line 57 to col. 10, line 5)**

7. As per **claims 15**, Bernasconi discloses "discarding a completion associated with the new request cycle received from the destination device" **(see col. 10, lines 50-60)**.

8. As per **claim 16,** Bernasconi discloses "a trigger-matching logic **(col. 9, lines 51-57, teaches that the trigger-matching logic is the logic that doest the matching between the current DSP program address and a break address correspond to a flawed DSP program stored in the ROM 18, such as at section 18b.)** to capture an incoming cycle **(col. 9, line 54 teaches the current DSP program address corresponds to the applicant incoming cycle)** and determine if the captured incoming cycle matches one or more of trigger conditions **(see col. 9, lines 51-57)**; and a control logic **(col. 9, lines 9, lines 57 to col. 10, line 5, teaches the that the control logic is taught by Bernasconi's patching circuitry 22, which carries out the steps of sending a branch op code to the DSP 16 followed by a branch address corresponding to the beginning of a block of corrected DSP program software in**

the RAM 20 such as in section 20b.) coupled to the trigger-matching logic to select a set of instructions upon detection of at least one matched trigger condition and to execute operations as specified by the selected set of instructions **(see fig. 1 and col. 9, line 57 to col. 10, line 5), Bernasconi also discloses**, "if the received incoming cycle matches a trigger condition and is a non-posted cycle **(col. 9, lines 51-57), the patching circuitry does** one of following (1) unmodified header information from the captured non-posted cycle **(see fig. 1 and col. 9, line 57 to col. 10, line 5)**, (2) modified header information associated with a modified non-posted cycle, or (3) header information associated with a new cycle generated in response the received incoming cycle.

Bernasconi fails to specifically teach specifying whether the I/O controller including a patch module **(patching circuitry22)** coupled to a completion queue is to be loaded with information from non-posted cycle. However, Hagan suggests interrupt state to be cleared when the entry is posted, the interrupt state being associated with each entry in the queue **(see abst. and col. 4, lines 47-59).**

Bernasconi's invention and Hagan's invention's are analogous art because they are from the same field of endeavor storing data into queue from a processor. In view of such teaching, at the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the patch mechanism used to detect and workaround defects and conditions existing in an integrated circuit chip as taught by Bernasconi which includes a DSP and a patching circuitry that's consist of a trigger-matching logic, further include a control logic coupled to the trigger-matching logic is modified to

include a completion queue to be loaded with information from non-posted cycle as taught by Hagan.

The motivation for doing so would have been because Hagan teaches that **["The significant instructions generally translate into increased processing time, slowing the response of the processor determining whether the current queue entry is empty. Therefore, it would be advantageous to have an improvement with an apparatus for reducing the processing overhead for multiple processor or embedded processor architectures in posting events or tasks to a queue"(col. 1, lines 49-56)]**.

Therefore, it would have been obvious to combine Hagan and Bernasconi for the benefit of creating a patch mechanism used to detect and workaround defects and conditions existing in an integrated circuit chip to obtain the invention as specified in claim 16.

9. As per **claim 17**, Bernasconi discloses "the system of claim 1,"**[see rejection to claim 1 above]** "wherein the trigger-matching logic and the control logic are incorporated within an Input/Output (I/O) chip **(with respect to this limitation, Bernasconi discloses the logic that doest the matching between the current DSP program address and a break address take place inside the patching circuitry 22 that is discloses in fig. 2. The patching circuitry 22 is shown in fig. 1 coupled to a control logic, incorporated within an Input/output (I/O) integrated circuit chip". (see fig. 1)**.

10. As per **claims 18 and 20**, Bernasconi discloses "wherein the control logic generates a modified non-posted, **which is a new request cycle**, based on the at least one matched trigger condition **(col. 9, lines 9, lines 57 to col. 10, line 5, teaches the that the control logic is taught by Bernasconi's patching circuitry 22, which carries out the steps of sending a branch op code to the DSP 16 followed by a branch address corresponding to the beginning of a block of corrected DSP program software in the RAM 20 such as in section 20b.);** sending the modified non-posted cycle to a destination device **(processor 16 in fig. 1)**.

11. As per **claim** 19, Bernasconi discloses "wherein the control logic **(col. 9, lines 9, lines 57 to col. 10, line 5, teaches the that the control logic is taught by Bernasconi's patching circuitry 22, which carries out the steps of sending a branch op code to the DSP 16 followed by a branch address corresponding to the beginning of a block of corrected DSP program software in the RAM 20 such as in section 20b.)** instructs a patch module to whether or not to return a completion associated with the modified non-posted cycle to the requesting device **(processor 16)**.

Bernasconi fails to specifically teach specifying whether the I/O controller including a patch module **(patching circuitry22)** coupled to a completion queue is to be loaded with information from non-posted cycle. However, Hagan suggests interrupt state to be cleared when the entry is posted, the interrupt state being associated with each entry in the queue **(see abst. and col. 4, lines 47-59).**

Bernasconi's invention and Hagan's invention's are analogous art because they are from the same field of endeavor storing data into queue from a processor. In view of

such teaching, at the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the patch mechanism used to detect and workaround defects and conditions existing in an integrated circuit chip as taught by Bernasconi which includes a DSP and a patching circuitry that's consist of a trigger-matching logic, further include a control logic coupled to the trigger-matching logic is modified to include a completion queue to be loaded with information from non-posted cycle as taught by Hagan.

The motivation for doing so would have been because Hagan teaches that **["The significant instructions generally translate into increased processing time, slowing the response of the processor determining whether the current queue entry is empty. Therefore, it would be advantageous to have an improvement with an apparatus for reducing the processing overhead for multiple processor or embedded processor architectures in posting events or tasks to a queue"(col. 1, lines 49-56)]**.

Therefore, it would have been obvious to combine Hagan and Bernasconi for the benefit of creating a patch mechanism used to detect and workaround defects and conditions existing in an integrated circuit chip to obtain the invention as specified in claim 19.

V. RELEVANT ART CITED BY THE EXAMINER

12. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See MPEP 707.05(c).

13. The following references teach a computer system used to detect, transfer data, workaround defects and conditions existing in an integrated circuit chip.

U.S. PATENT NUMBER

US 2004/0237009
US 6,463,549
US 6,314,024

VI. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

14. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

ALLOWABLE SUBJECT MATTER

15. The following is an examiner's statement of reasons for allowance: In regards to claims 1-10, the prior art of record fails to disclose "instructing the completion queue whether or not to discard a completion packet received from a designated end-device". The remaining claims 2-9 are allowed by virtue of their dependencies on the independent claims. Hence, the examiner has allowed claims 1-10.

a(1) CLAIMS REJECTED IN THE APPLICATION

16. Per the instant office action, claims 1-24 have received a final action on the merits.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

b. DIRECTION OF FUTURE CORRESPONDENCES

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ernest Unelus whose telephone number is (571) 272-8596. The examiner can normally be reached on Monday to Friday 9:00 AM to 5:00 PM.

IMPORTANT NOTE

18. If attempts to reach the above noted Examiner by telephone is unsuccessful, the Examiner's supervisor, Mr. Fritz M. Fleming, can be reached at the following telephone number: Area Code (571) 272-4145.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

August 23, 2006

Ernest Unelus
Examiner
Art Unit 2181

KIM HUYNH
SUPERVISORY PATENT EXAMINER
8/28/06